

August 1998 - Revised May 2000

## 4-Bit Binary Fill Adder With Fast Carry

### Features

- Buffered Inputs
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption
- Balanced Propagation Delays
- AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply
- ±24mA Output Drive Current
  - Fanout to 15 FAST™ ICs
  - Drives 50Ω Transmission Lines

### Description

The 'AC283 and 'ACT283 4-bit binary adders with fast carry that utilize Advanced CMOS Logic technology. These devices add two 4-bit binary numbers and generate a carry-out bit if the sum exceeds 15.

Because of the symmetry of the add function, this device can be used with either all active-HIGH operands (positive logic) or with all active-LOW operands (negative logic). When using positive logic, the carry-in input must be tied LOW if there is no carry-in.

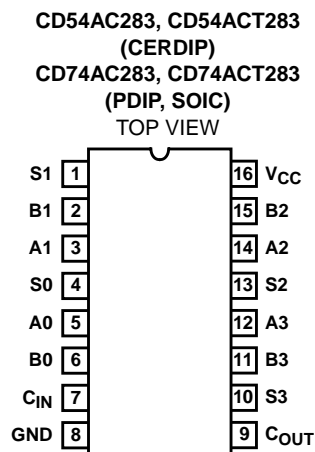
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54AC283F3A	-55 to 125	16 Ld CERDIP
CD74AC283E	0 to 70°C, -40 to 85, -55 to 125	16 Ld PDIP
CD74AC283M	0 to 70°C, -40 to 85, -55 to 125	16 Ld SOIC
CD54ACT283F3A	-55 to 125	16 Ld CERDIP
CD74ACT283E	0 to 70°C, -40 to 85, -55 to 125	16 Ld PDIP
CD74ACT283M	0 to 70°C, -40 to 85, -55 to 125	16 Ld SOIC

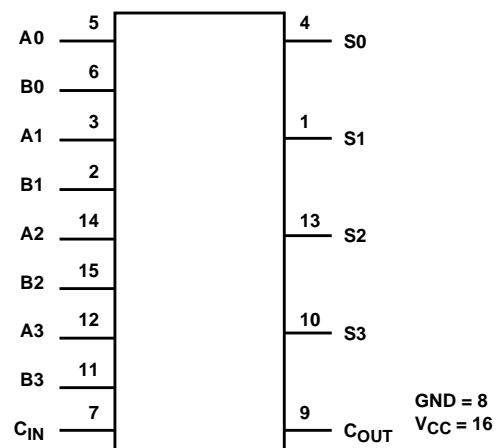
#### NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

### Pinout



### Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

## CD54/74AC283, CD54/74ACT283

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 6V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 50mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 50mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ (Note 3) .....	$\pm 100mA$

### Thermal Information

Thermal Impedance (Typical, Note 5)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	67 $^{\circ}C/W$
SOIC Package .....	73 $^{\circ}C/W$
Maximum Junction Temperature (Plastic Package) .....	150 $^{\circ}C$
Maximum Storage Temperature Range .....	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	300 $^{\circ}C$

### Operating Conditions

Temperature Range, $T_A$ .....	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$ (Note 4)	
AC Types .....	1.5V to 5.5V
ACT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Slew Rate, dt/dv	
AC Types, 1.5V to 3V .....	50ns (Max)
AC Types, 3.6V to 5.5V .....	20ns (Max)
ACT Types, 4.5V to 5.5V .....	10ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTES:

3. For up to 4 outputs per device, add  $\pm 25mA$  for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5. The package thermal impedance is calculated in accordance with JESD 51.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$		-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	MAX	MIN	MAX	MIN	MAX		
<b>AC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	1.5	1.2	-	1.2	-	1.2	-	V	
				3	2.1	-	2.1	-	2.1	-	V	
				5.5	3.85	-	3.85	-	3.85	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	1.5	-	0.3	-	0.3	-	0.3	V	
				3	-	0.9	-	0.9	-	0.9	V	
				5.5	-	1.65	-	1.65	-	1.65	V	
High Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	-4	3	2.58	-	2.48	-	2.4	-	V
			-24	-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	-75	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	-50	5.5	-	-	-	-	3.85	-	V

**CD54/74AC283, CD54/74ACT283**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS	
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	MAX	MIN	MAX	MIN	MAX		
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	12	3	-	0.36	-	0.44	-	0.5	V
			24	24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	μA	
Quiescent Supply Current MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	8	-	80	-	160	μA	
<b>ACT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	2	-	2	-	V	
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V	
High Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	μA	
Quiescent Supply Current MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	8	-	80	-	160	μA	
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA	

**NOTES:**

6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
7. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

**ACT Input Load Table**

INPUT	UNIT LOAD
A0, B0, A2, B2	1.66
A1, B1	1.9
A3, B3	1.4
C <sub>IN</sub>	1.1

NOTE: Unit load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

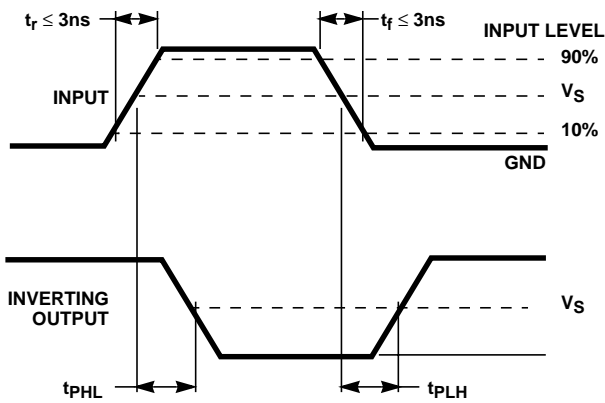
## CD54/74AC283, CD54/74ACT283

### Switching Specifications Input $t_r, t_f = 3\text{ns}$ , $C_L = 50\text{pF}$ (Worst Case)

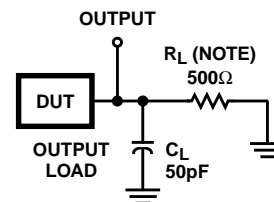
PARAMETER	SYMBOL	$V_{CC}$ (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>AC TYPES</b>									
Propagation Delay, An or Bn to $C_{OUT}$ $C_{IN}$ to Sn $C_{IN}$ to $C_{OUT}$	$t_{PLH}, t_{PHL}$	1.5	-	-	199	-	-	219	ns
		3.3 (Note 9)	6.3	-	22.4	6.2	-	24.6	ns
		5 (Note 10)	4.5	-	16	4.4	-	17.6	ns
Propagation Delay, An or Bn to Sn	$t_{PLH}, t_{PHL}$	1.5	-	-	207	-	-	228	ns
		3.3	6.6	-	23.2	6.4	-	25.5	ns
		5	4.7	-	16.5	4.6	-	18.2	ns
Input Capacitance	$C_I$	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	120	-	-	120	-	pF
<b>ACT TYPES</b>									
Propagation Delay, An or Bn to $C_{OUT}$ $C_{IN}$ to Sn $C_{IN}$ to $C_{OUT}$	$t_{PLH}, t_{PHL}$	5 (Note 10)	4.5	-	16	2.7	-	17.6	ns
		5	4.7	-	16.5	3.3	-	18.2	ns
Input Capacitance	$C_I$	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	120	-	-	120	-	pF

**NOTES:**

8. Limits tested 100%.
9. 3.3V Min is at 3.6V, Max is at 3V.
10. 5V Min is at 5.5V, Max is at 4.5V.
11.  $C_{PD}$  is used to determine the dynamic power consumption per function.  
 AC:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$   
 ACT:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.



**FIGURE 1. PROPAGATION DELAY TIMES**



NOTE: For AC Series Only: When  $V_{CC} = 1.5\text{V}$ ,  $R_L = 1\text{k}\Omega$ .

	AC	ACT
Input Level	$V_{CC}$	3V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

**FIGURE 2. PROPAGATION DELAY TIMES**

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD54AC283F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54ACT283F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD74AC283E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74AC283EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74AC283M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC283M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC283M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC283M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC283ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC283MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT283E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT283EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT283M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT283M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT283M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT283M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT283ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT283MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC283M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74ACT283M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC283M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74ACT283M96	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

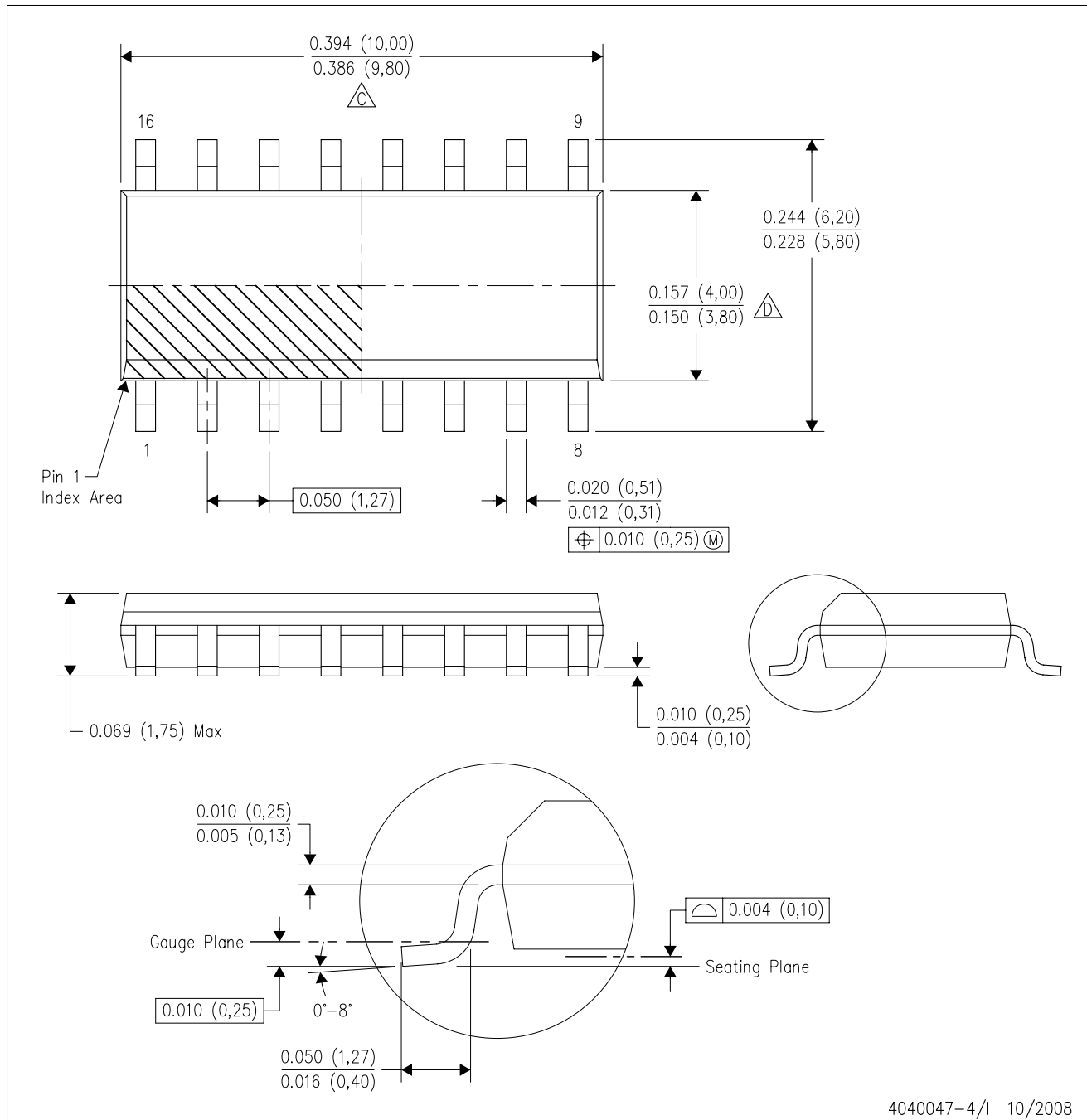


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- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

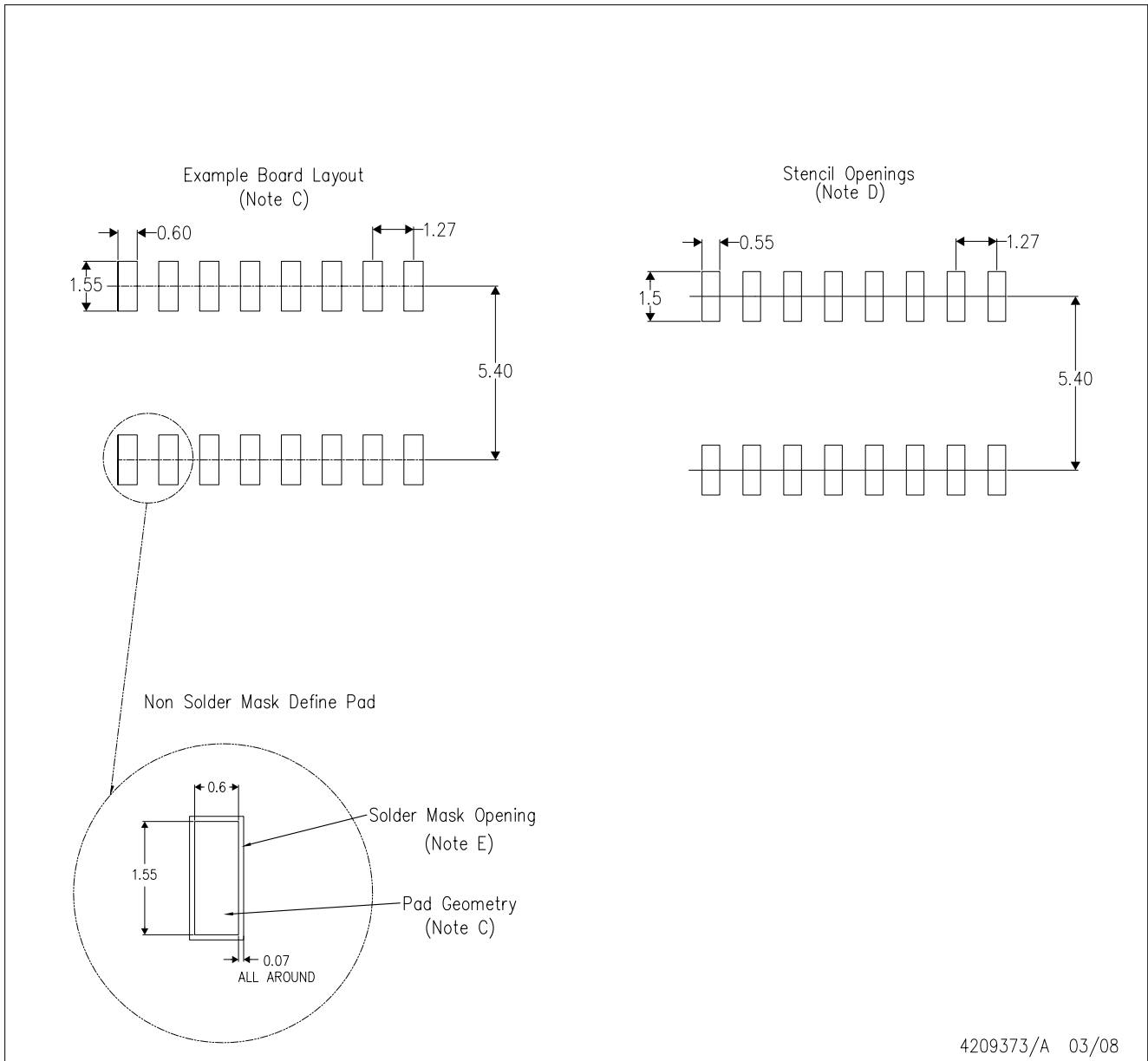
D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.